ABSTRACT OF THE INVENTION

A current steering digital-to-analog (DAC) having improved dynamic performance and output signal quality (i.e. improved SFDR characteristic). The DAC includes current steering segments each having differential transistors to steer a current from a summing node to either the positive or negative output. The DAC further comprises a control circuit to reduce the variation of the voltage present at each summing node. More specifically, the control circuit includes a first circuit that controls the threshold voltage of the corresponding differential transistors that are electrically connected to the positive output in response to the sensed positive output voltage such that the voltages at the corresponding summing nodes remain constant. Similarly, the control circuit includes a second circuit that controls the threshold voltage of the differential transistors that are electrically connected to the negative output in response to the sensed negative output voltage such that the voltages of the corresponding summing nodes remain constant.